IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETLIST, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 1:22-cv-00134-LY **JURY TRIAL DEMANDED**
NETLIST, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 1:22-cv-00136-LY **JURY TRIAL DEMANDED**

PLAINTIFF NETLIST, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF REGARDING U.S. PATENT NOS. 8,301,833; 9,824,035; 10,268,608; AND 10,489,314

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Cases

Other Authorities

TABLE OF EXHIBITS

Exhibit	Description
A.	*Curriculum Vitae* of Steven Przybylski, Ph.D.
B.	JEDEC Standard – JESD79-2A
C.	JEDEC Standard – JESD79-2B
D.	*Synchronous DRAM Architectures, Organizations, and Alternative Technologies*, by Prof. Bruce L. Jacob, December 10, 2002
E.	Wiley Electrical and Electronics Engineering Dictionary (2004)
F.	U.S. Patent No. 9,081,718 to Reche

Plaintiff Netlist, Inc. ("Netlist") hereby submits its Responsive Claim Construction Brief for United States Patent Nos. 8,301,833 ("'833 Patent"); 9,824,035 ("'035 Patent"); 10,268,608 ("'608 Patent"); and 10,489,314 ("'314 Patent") (collectively, the "Asserted Patents").

I. THE COURT SHOULD ADOPT NETLIST'S CONSTRUCTIONS

Netlist proposes constructions that adhere to the well-known principles of claim construction, are based on the plain and ordinary meaning of the claim terms, and are founded on the teachings of the intrinsic evidence. Micron, on the other hand, proposes constructions with an eye toward manufacturing validity defenses and impermissibly limiting claim scope. For example, Micron repeatedly proposes that claim terms lacking the term "means" be construed as means-plus-function limitations, flat-out ignoring intrinsic structural disclosures. Micron also seeks to narrow terms without demonstrating a clear disavowal of claim scope. As such, Netlist respectfully requests the Court adopt its proposed constructions and reject Micron's proposals.

II. CLAIM CONSTRUCTION REGARDING THE '833 PATENT

Volatile memories (*e.g.*, DRAM) lose data when power is removed. Non-volatile memories (*e.g.*, flash memory) retain their data when power is removed. The '833 Patent teaches a memory system where data can be transferred between a volatile memory subsystem and non-volatile memory subsystem. '833 Patent at 3:64-67; 17:49-67. Such transfers allow data in the faster volatile memory to be backed up to the slower, but persistent, non-volatile memory, and then restored from the non-volatile memory to the volatile memory. *Id*. at 10:33-37.

A. "volatile memory subsystem"; "non-volatile memory subsystem" (Claim 15)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure.	"volatile memory subsystem" means "one or more volatile memory devices." "non-volatile memory subsystem" means "one or more non-volatile memory devices."

The dispute here concerns the word "subsystem." A POSITA would understand the plain and ordinary meaning of a memory "subsystem" is part of a larger system. Declaration of Steven Przybylski ("Przybylski Decl."), ¶ 32. That concept would be readily understood by a lay person and needs no construction. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) ("[T]he ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges…"). Despite the recognized plain and ordinary meaning of "subsystem," Micron seeks to replace "subsystem" with "devices"—eliminating the inherent systemic descriptor found in "subsystem" and narrowing the subsystem to only "devices." That is improper. *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1344 (Fed. Cir. 2009) (claims must not be redrafted).

A POSITA would understand that a memory subsystem can be broader than a memory device and include other components or elements such as registers, data interconnects and/or control elements. Przybylski Decl., ¶ 33. This is consistent with the specification's teachings. *See, e.g.*, '833 Patent at 7:8-11 ("the volatile memory subsystem 30 can comprise a registered DIMM subsystem comprising one or more registers"); 18:14-29 ("data lines," "chip select lines," and "self-refresh lines" part of a volatile memory subsystem); 18:33-44 (disclosing "volatile memory subsystem data bus"). Micron impermissibly narrows claim scope without identifying any clear disavowals in the specification. Micron's proposed constructions must be rejected. *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019) ("[T]he specification must contain expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.") (quotations omitted).

Micron further argues that the claims must be rewritten (1) to "stay true to the claim language," and (2) because "[t]he '833 Patent consistently describes the volatile/non-volatile

memory subsystem as a series of memory elements and refers to other components on the memory system as something different." Dkt. 41 ("Brief") at 4. The best way to stay true to the claim language is to not rewrite it. Micron relies on select aspects of Figure 1 to support its narrowing proposals, but even Figure 1 depicts memory devices ***and*** interconnects (*e.g.*, data buses) as part of the memory subsystems. *See* Przybylski Decl., ¶ 33. Figure 1 also represents a single, non-limiting embodiment. *See Continental Circuits*, 915 F.3d at 797 (claim scope cannot be limited based on specification's non-limiting embodiments). Micron's reliance on Figure 1 to limit claim scope is therefore misplaced.

Micron also argues that the prosecution history supports its proposals. Not so. Netlist's annotated reproductions of Figure 1 in prior IPR proceedings fall far short of clear or unmistakable disavowal of claim scope. In fact, after referencing annotated Figure 1, Netlist proposed that the plain and ordinary meaning of a "memory subsystem" would be a "part of a larger memory system," and *expressly rejected* Petitioner's construction that "would narrow the subsystem to include 'two or more memory components' and nothing else." Dkt. 41-18 (Ex. 16 to Stone Decl.) at 12, 17-19. Notably, Micron's proposed construction is essentially the same as Petitioner's narrow construction of "memory subsystems" rejected by the PTAB. Dkt. 41-19 (Ex. 17 to Stone Decl.) at 5. Moreover, Netlist distinguished prior art memory subsystems on technical grounds, and not on a narrow construction of "subsystems" excluding all other elements. *See, e.g., id.* at 52-58; Dkt. 41-16 (Ex. 14 to Stone Decl.) at 21 (distinguishing prior art while arguing "FLASH ***controller*** section 30 is ***(correctly)*** recognized as being ***part of a non-volatile memory subsystem***") (emphasis added). Thus, the PTAB's IPR decisions were not based

on Netlist's alleged representations limiting claim scope.[1]

Micron also points to Netlist's statements in an IPR preliminary response that the volatile and non-volatile memory subsystems "*may comprise* one or more" memory elements. Brief at 5. But these statements are not a clear or unmistakable disavowal of claim scope, and the open-ended term "comprise" indicates subsystems are not limited to just "memory devices." *See, e.g., Visual Intel. LP v. Optech, Inc.*, No. H-13-2612, 2015 WL 851970, at *5 (S.D. Tex. Feb. 26, 2015) (statement that imaging sensors "may comprise" passive sensors was not disavowal of active sensors). The Court should give the "subsystem" terms their plain and ordinary meaning.

B. "controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation" (Claim 16)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Not subject to § 112, ¶ 6.	This is a means-plus-function limitation. Function: entire limitation after "configured to." Corresponding Structure: "controller that is separate from the volatile and non-volatile memory subsystems," as described in the '833 Patent, 6:63-7:40.

Claim 16 recites "controller" without the word "means." The claim language conveys sufficient structure to preclude application of § 112, ¶ 6. *Williamson*, 792 F.3d at 1348.

The Federal Circuit has held that § 112, ¶ 6 does not apply when terms are claimed together with language that connotes structure. *Linear Tech. Corp. v. Impala Linear Corp.*, 379

[1] Micron's citation to the *Sandisk* Decision is misplaced. Brief at 5. The PTAB did not deny institution based on a narrow construction of memory subsystems, but because Petitioner failed to "sufficiently explain what it considers the volatile memory subsystem and does not point to any clock with provides a first or third frequency to that subsystem." Dkt. 41-17 (Ex. 15 to Stone Decl.) at 12.

F.3d 1311, 1320 (Fed. Cir. 2004) ("[W]hen [a] structure-connoting term 'circuit' is coupled with a description of the circuit's operation…§ 112 ¶ 6 presumptively will not apply."). Here, claim 16 connotes sufficiently definite structure for "controller" to a POSITA because it describes the controller's operation: "configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation." '833 Patent at 22:12-17; Przybylski Decl., ¶ 39. The claim's description of the controller's operation is sufficient to avoid § 112, ¶ 6. *See, e.g., 911EP v. Whelen Eng'g Co*., 512 F. Supp. 2d 713, 727 (E.D. Tex. 2007) ("The claim language…***adds further structure by describing the operation of the controller***… sufficient to avoid section 112, ¶ 6.") (emphasis added).

Moreover, a POSITA would understand that the claimed "controller" refers to a known class of memory technology components that can coordinate and control memory operations, couple and decouple disparate memory types with different interfaces and data flow patterns, produce outputs in response to inputs, and format or process data. *See* Przybylski Decl., ¶ 40.[2] This is taught by the '833 Patent's specification. *See, e.g.,* '833 Patent at 2:46-49; 4:58-61; 4:63-64; 6:55-59; 6:63-7:4; 7:8-40; 8:22-31; 8:31-36; 10:8-18; 15:46-16:3. For example, the specification teaches that the "controller" regulates data flow. *See, e.g*., *id*. at 2:53-56 ("***controller configured to allow data to be communicated*** between the volatile memory subsystem and the host system") (emphasis added); 8:28-31; 10:15-17; 10:19-22; *see also* Przybylski Decl., ¶ 40. The specification further teaches that "other management capabilities [for the] non-volatile memory subsystem 40 are performed in the controller," and the "controller" is

[2] Indeed, Micron's own patents (*e.g*., U.S. Patent No. 9,081,718) recognize that controllers are physical components capable of inputting data and outputting data, and of being able to "control and communicate" with memory devices. *See* Przybylski Decl., ¶ 42.

described as having various potential configurations, such as an FPGA. *See, e.g., id*. at 6:54-59, 10:55-58, 15:47-54.

Micron's assertion that "controller" is a nonce word also fails. Brief at 7. Micron ignores the numerous cases finding that "controller" is ***not*** a nonce term. *See, e.g.*, *Virginia Innovation Scis., Inc. v. Amazon.com, Inc*., No. 4:18-cv-474, 2019 WL 4259020, at *13 (E.D. Tex. Sep. 9, 2019) (rejecting argument that controller is a nonce term); *Barkan Wireless IP Holdings, L.P. v. Samsung Elecs. Co*., No. 2:18-cv-28-JRG, 2019 WL 497902, at *22 (E.D. Tex. Feb. 7, 2019) (same); *Sound View Innovations, LLC v. Facebook, Inc*., No. 16-cv-116 (RGA), 2017 WL 2221177, at *5 (D. Del. May 19, 2017) (same); *Maxell Ltd. v. Huawei Device USA Inc*., 297 F. Supp. 3d 668, 748 (E.D. Tex. 2018) (same).

Micron's reliance on *MTD Prods. Inc. v. Iancu*, 933 F.3d 1336, 1343 (Fed. Cir. 2019) is also misplaced. There, the disputed term "mechanical control assembly" was not disclosed in the specification, and had no well-understood meaning in the art. *Id*. at 1340, 1344. Thus, the Federal Circuit held that the term was not governed by § 112, ¶ 6. Here, in contrast, the '833 Patent describes the claimed "controller" in detail, and a POSITA would understand what is meant by "controller" in the '833 Patent claims. *See* Przybylski Decl., ¶¶ 39-41.

Micron's reliance on *Incom Corp. v Radiant RFID, LLC*, No. 1-17-cv-0009-LY, 2018 WL 4690934, at *5 (W.D. Tex. Sep. 28, 2018) is similarly misplaced. There, the court concluded "'tag orientation controller' does not name particular structures described in the specification, but rather 'refers only to a general category of whatever may perform specified functions,'" unlike cases in which "the patent provided a detailed description of the structure of the disputed term by name." *Id*. at *6 (citing cases). The '833 Patent describes the claimed "controller" in detail, by name, and conveys definite structure, and this case is distinguishable from *Incom*.

Even if Micron can overcome the presumption that § 112, ¶ 6 does not apply, "controller" should be construed to encompass the embodiments disclosed in the '833 Patent for performing the claimed function. *See, e.g.*, '833 Patent at 15:47-54 (FPGA); *see also* 2:46-49; 2:53-56; 4:58-61; 4:63-64; 6:55-59; 8:28-31; 10:8-22; 10:55-58; Przybylski Decl., ¶¶ 40-41. Micron argues that "controller" should be limited to one embodiment, which Micron contends is a "controller that is separate from the volatile and non-volatile memory systems." But the tenets of claim construction prohibit limiting claim scope to a single disclosed embodiment. The '833 Patent never teaches that the controller *must* be separate and distinct from the non-volatile memory subsystem or the volatile memory subsystem. *See Continental Circuits*, 915 F.3d at 797. And volatile and non-volatile memory subsystems may or may not include certain types of control elements. *See supra,* Section II.A. Thus, Micron's narrow construction finds no support in the specification and should be rejected.

III. CLAIM CONSTRUCTION REGARDING THE '035 AND '608 PATENTS

The '608 Patent is a continuation of the '035 Patent. Both patents are directed to memory modules that ensure proper timing of the control and data signals received and transmitted between the memory modules and a processor. The claims read on memory modules that include a module control device that receives and transmits command signals, memory devices that perform memory operations in response to signals sent by the module control device, and data buffers that include logic for obtaining timing information from a memory operation and controlling timing of data and strobe signals on data paths based on that timing information.

A. "module control device"[3]

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Neither indefinite nor subject to § 112, ¶ 6.	This is a means-plus function limitation. Function: entire limitation after "configured to." Corresponding Structure: Indefinite – no corresponding structure.

Claim 1 recites "a module control device" without the word "means." The claim language conveys sufficient structure to preclude application of § 112, ¶ 6. *Williamson*, 792 F.3d at 1348.

The claims require that the "module control device" must be "mounted on the module board." '035 Patent at claim 1; '608 Patent at claim 1. The claims further describe that the "module control device" be configured to (1) receive certain signals for a particular operation from the memory controller via specified signal lines; and (2) output specific signals in response. *Id*. Performance of these functions requires certain structural capability that cannot be achieved by any generic hardware or software component. Przybylski Decl., ¶ 56; *see also Linear Tech.*, 379 F.3d at 1320; *Abacus*, 462 F.3d at 1355-56.

For example, a POSITA would understand that the claims require that the "module control device" have (1) connections to signal traces for receiving commands from a memory controller; (2) connections to command signal traces that couple the module control device to other components on the memory module; and (3) internal functional units responsible for registering and decoding the command signals and the driving of the module control signals and the module command signals, respectively. *Id.* at ¶¶ 58-59. A POSITA would also understand that many control structures and implementations are outside the scope of the claimed term; for example, the claims would exclude from the scope of the claimed "module control device" the

[3] The full term is included in Micron's Opening Brief.

host memory controller, or other controllers that may be on module but exclusively perform non-data related control functions (for example, controllers for power supply or engine). *Id.* at ¶ 61.

Micron wrongly suggests that the claim language does not describe how the "module control device" interacts with other claim components; this ignores the express claim language. For example, claim 1 of the '035 Patent provides that the "module control device" must receive memory command signals *from the memory controller via control/address signal lines*. Przybylski Decl., ¶ 60. The claims also recite that the "module control device" outputs module command signals and module control signals *to memory devices and buffer circuits*, respectively. '035 Patent at claim 1; '608 Patent at claim 1; Przybylski Decl., ¶ 60. Thus, the claim language provides details regarding how the "module control device" "interacts with other components ... in a way that ... inform[s] the structural character of the limitation-in-question or otherwise impart[s] structure...." *Williamson*, 792 F.3d at 1351.

Ignoring the claim language as written, Micron argues that § 112, ¶ 6 must apply because the words "module," "control," and "device"—viewed only in isolation—are nonce words lacking structure for performing the claimed function. But Micron has not asked the Court to construe the terms individually, and terms must be construed in context. *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999) ("Proper claim construction, however, demands interpretation of the entire claim in context, not a single element in isolation."). Micron's analysis that focuses on individual terms in a vacuum is inapposite because the explicitly defined structure makes clear that the patentee *here* did not recite those terms as generic nonce words in *these particular claims*. Micron relies on *Williamson*, but again its reliance is misplaced. In *Williamson*, the Federal Circuit concluded "module" was a nonce word because, as claimed in that case, it did "not provide any indication of structure" but instead "set

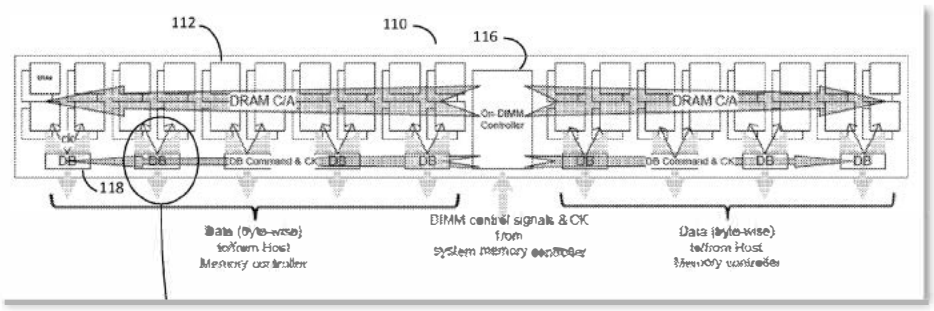
forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used." 792 F.3d at 1350. Here, as described above, the claim language inarguably indicates well-defined structure.

The claims' recitation of the term "module" as a modifier of "control device" does not reflect the patentee's reliance on a generic nonce word as Micron argues. Instead, "module" is a specific reference to the patents' extensive disclosure of *memory modules*, which connote a specific, structural meaning to a POSITA. *See, e.g.,* '035 Patent at 1:40-2:32 ("A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB)."), 8:6-9 ("In certain embodiments, the memory module 110 is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM)."); *see also* '608 Patent at 1:50-2:36, 8:9-12; Przybylski Decl., ¶ 62. This is reflected in the language of Claim 1 itself, which claims "[a] memory module…" that the claimed "module control device" is a part of. Micron's attempt to decouple the disputed term from the context of the claims and specification must be rejected.

Micron also completely ignores the specification's extensive description of the structure of the "module control device."[4] The "module control device" 116 is "coupled to the [memory controller] 101 via the C/A signal lines," and "the memory devices 112, the module control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119." '035 Patent at 4:25-33; '608 Patent at 4:27-35;

[4] The specification also refers to the "module control device" 116 as a "module control circuit" or a "module controller." *See* '035 Patent at 4:25-30; '608 Patent at 4:27-32.

Przybylski Decl., ¶¶ 62-63. The specifications also describe that "[i]n certain embodiments, the control circuit 116 includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain." '035 Patent at 8:9-12; '608 Patent at 12-16; Przybylski Decl., ¶¶ 62-63. The specifications also describe how the module control signals "travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118." '035 Patent at 9:49-54; '608 Patent at 9:52-57; Przybylski Decl., ¶¶ 62-63. Indeed, Figure 2D shows a physical "module control device" (116) on the memory module, between sets of memory devices and having certain signaling pathways:



Przybylski Decl., ¶¶ 62-63.

Even if Micron overcomes the presumption that § 112, ¶ 6 does not apply, the specification discloses corresponding structure. "Module control device" should be construed to encompass each of the embodiments disclosed in the '035 and '608 Patents for performing the claimed function. *See* '035 Patent Figures 1, 2A, 2B, 2C, 2D, 7, 12A, 12B, 4:25-33; 4:63-5:8; 5:55-63, 8:6-30; *see also* '608 Patent at Figures 1, 2A, 2B, 2C, 2D, 7, 12A, 12B, 4:27-35; 4:65-5:10, 5:58-66, 8:9-34; *see also Creo Prods., Inc. v. Presstek, Inc.*, 305 F.3d 1337, 1346 (Fed. Cir. 2002) ("Proper application of § 112, ¶ 6 generally reads the claim element to embrace distinct and alternative described structures for performing the claimed function.") (citations omitted); *see also* Przybylski Decl., ¶ 65. Micron's erroneous proposed construction must be rejected.

B. "logic configured to respond to the module control signals by enabling the data paths . . . wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation to control timing of the respective data and strobe signals on the data paths in accordance with the timing information" ('035 Patent, Claim 1)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Neither indefinite nor subject to § 112, ¶ 6.	This is a means-plus function limitation. Function: entire limitation after "configured to." In addition, the entire limitation after "the logic is further configured to." Corresponding Structure: Indefinite – no corresponding structure.

Again, Micron attempts to shoehorn a structural claim term into the confines of § 112, ¶ 6. But courts have consistently found that the term "logic" connotes sufficiently definite structure and is not a "nonce" or "functional" word that is subject to the limitations of § 112, ¶ 6. *See, e.g.*, *CDN Innovations, LLC v. Grande Commc'ns Networks, LLC*, 2021 WL 3615908, at *11-12 (E.D. Tex. Aug. 13, 2021); *Uniloc USA, Inc. v. Samsung Elecs. Am., Inc.*, No. 2:17-cv-651-JRG, 2018 WL 5296046, at *18 (E.D. Tex. Oct. 24, 2018) (concluding that the term "incline logic" was not subject to 35 U.S.C. § 112 ¶ 6 and did not require construction); *TecSec, Inc. v. IBM*, 731 F.3d 1336, 1348 (Fed. Cir. 2013) ("[T]he term 'digital logic' designates structure to skilled artisans—namely digital circuits that perform Boolean algebra."); *Intel Corp v. VIA Techs.*, 319 F.3d 1357, 1366 (Fed. Cir. 2003) (finding that "core logic" was adequate corresponding structure for a claimed function even though there was no specific circuitry disclosed to show how the "core logic" was modified); *Razor USA LLC v. DGL Grp.*, No. 19-12939(JMV), 2021 WL 651257, at *19 (D.N.J. Feb. 19, 2021) (finding that 35 U.S.C. § 112, ¶ 6 did not apply and construing "control logic" as "electronic control circuitry"); *PCTEL, Inc. v. Agere Sys.*, No. C 03-2474 MJJ, 2005 WL 2206683 at *21 (N.D. Cal. Sep. 8, 2005) ("A review

of the technical dictionaries supports [patentee]'s view that 'logic,' by itself, can connote structure.") (citing McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed. 1994)).

Micron wholly ignores the universe of cases that doom its position. And the single case relied on by Micron is inapplicable here because, in *Egenera Inc. v. Cisco Sys.*, the term "logic to modify . . ." appeared in claims that broadly covered a software platform, and the functionality described in the claim did not convey any structure to a POSITA. 972 F.3d 1367, 1375 (Fed. Cir. 2020). Importantly, the *Egenera* court drew a distinction between logic claimed as "circuitry"—which does convey sufficient structure—and logic claimed as an abstract concept referring to computer operations generally, which does not. *Id.* The district court in that case concluded that a POSITA would not understand "logic" as claimed in that patent to refer to circuitry, but rather as an abstraction for the set of steps designed to accomplish a stated function, and the court applied § 112, ¶ 6. *Egenera, Inc. v. Cisco Sys., Inc.*, No. 16-11613-RGS, 2018 WL 717342, at *5 (D. Mass. Feb. 5, 2018), *aff'd*, 972 F.3d 1367 (Fed. Cir. 2020). On appeal, the Federal Circuit agreed, finding that the claims provided "no structural limitation to the 'inputs, outputs, connections, and operation' of the claimed 'logic to modify,'" and, on that basis, held that "logic" as claimed was a generic substitute for the word "means." *Egenera*, 972 F.3d at 1375.

Here, in contrast, the use of the term "logic" in the context of memory modules and as claimed, specifically, conveys sufficient structure to a POSITA. Przybylski Decl., ¶ 69. The claims do not recite "logic" as an abstract concept. Instead, they describe the objectives and operations of the circuitry, which includes a memory module including a buffer circuit with logic that is configured to respond to *particular* signals generated from *particular* structural components, obtain timing information during *particular* operations, and then control timing of *particular* signals traveling along a *particular* data path. *See* '035 Patent at claim 1; Przybylski

Decl., ¶ 70. Specifically, the "logic" claimed in the '035 Patent must be configured to (1) respond to module control signals, which are generated—in response to a first memory operation from a system memory controller—by a module control device mounted on the module board and sent to buffer circuits that are positioned between data/strobe signal lines and a set of memory devices; (2) enable data paths that are used to transfer data and strobe signals between the set of memory devices and the system memory controller; (3) obtain timing information via signals received by a buffer circuit during a memory operation; and (4) control timing of data and strobe signals on the data paths based on the timing information. '035 Patent at claim 1; Przybylski Decl., ¶ 70.

Unlike in *Egenera*, the functions attributed to the claimed "logic" in the '035 patent cannot be performed by a generic, black-box software component. Przybylski Decl., ¶ 71. Instead, a POSITA would understand that "logic" refers here to particular control, data, and timing circuitry, which courts have consistently found to convey sufficient structure. *Id.* For example, a POSITA would understand that the claimed "logic" in the recited buffer circuit would include (1) logic circuitry that performs logic operations to obtain timing information based on the signals received by the buffer circuit; and (2) control circuitry to control the timing of the data and strobe signals on the data paths in the buffer circuit. *Id.* The "logic" would also enable the data paths within the buffer circuit in response to the module control signals. The "logic" would also include a decoder to interpret the module control. *Id.* These constraints ground the "logic" term and belie Micron's claims of abstraction.

A POSITA would further understand that certain logic structures and implementations are outside the scope of the claimed "logic." For example, because the claimed "logic" is included in the buffer circuit to control data transfers between the memory devices and the

memory controller, a POSITA would understand "logic" as circuitry capable of performing logic functions, and would understand that the claims would exclude any implementation of the claimed "logic" that is not circuitry capable of performing logic functions. *Id.* at ¶ 72. As a result, the term "logic" as recited in claim 1 designates structure to skilled artisans. *Id.* at ¶ 77.

Micron summarily asserts that the specification does not describe the structure of the buffer circuit's "logic." This is wrong. For example, the specification describes the isolation/buffer circuit 118, and teaches the use of logic circuits to deal with the difficulties of high-speed operation and the requirement for precise timing of the data and strobe signals. *See, e.g.,* '035 Patent at Figures 6, 8-19, 4:18-33; 8:1-5; and 8:18-30; Przybylski Decl., ¶¶ 73-75. The specification further describes how the module control signals are received and decoded, and how a logical mode signal can specify how the buffer circuit data path is to be enabled. '035 Patent at 5:40-48; Przybylski Decl., ¶¶ 73-75. The specification further describes, in Figure 6 and its associated text, the logic circuits found in certain embodiments of the buffer circuit. *Id*. at Figure 6, 11:66-12:34. The circuits that perform the temporal adjustment of the module control signals to avoid metastability are disclosed in detail, as well. *Id*. at 12:34-15:11; Przybylski Decl., ¶¶ 73-75.[5]

In determining the applicability of § 112, ¶ 6, the Court must determine whether the stated objectives and operation of the "logic" ***recited in the claims*** connote sufficiently definite structure. *Linear Tech.*, 379 F.3d at 1319-21 (Fed. Cir. 2004) (finding that "circuit [for performing a function]" was sufficiently definite structure because the claim recited the

[5] Technical dictionaries also confirm that use of the term "logic," by itself, connotes structure. *See, e.g*., Przybylski Decl., ¶ 76, Ex. E (defining "logic" as "[t]he circuits in a computer which enable the performance of logic functions or operations, such as AND, OR, and NOT. These include gates and flipflops. Also the manner in which these circuits are arranged.").

"objectives and operations" of the circuit.). Here, because a POSITA would understand "logic" as claimed in the '035 Patent to refer to circuitry, and that "logic" is not an abstract reference for generic computer operations, § 112, ¶ 6 does not apply.

Even if the Court determines that "logic" is a means-plus-function term in contravention of well-trodden caselaw and the intrinsic evidence here, the term still should be construed to encompass each of the embodiments disclosed in the '035 Patent for performing the claimed function. *See* '035 Patent at Figures 3, 6, 11A, 11B, 12A, 12B, 14, 15, 16, 19; *see id.* at 10:47-66, 12:7-22, 14:52-17:49, 18:9-15, and 18:63-19:7; Przybylski Decl., ¶ 78.

C. "a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal . . . at least one tristate buffer controlled by the command processing circuit" ('608 Patent, Claim 1)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Neither indefinite nor subject to § 112, ¶ 6.	This is a means-plus function limitation. Function: entire limitation after "configured to" and before "and a delay circuit." Corresponding Structure: Indefinite – no corresponding structure

As explained above, the Federal Circuit has made clear that where the term "circuit" is "combined with a description of the function of the circuit, [it] connote[s] sufficient structure to one of ordinary skill in the art to avoid §112, ¶ 6 treatment." *Abacus,* 462 F.3d at 1355-1356 (finding the recitation of "aesthetic correction circuitry" sufficient to avoid § 112, ¶ 6, treatment because the term circuit, combined with a description of the function of the circuit, connoted sufficient structure to one of ordinary skill in the art); *see also Linear Tech.*, 379 F.3d at 1319-21 (finding that "circuit [for performing a function]" was sufficiently definite structure because the claim recited the "objectives and operations" of the circuit); *Apex Inc. v. Raritan Computer, Inc.*,

325 F.3d 1364, 1373 (Fed. Cir. 2003) ("[T]he term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art."). The Federal Circuit has consistently declined to interpret the terms like, "logic, "circuit," or "circuitry" as means-plus-function limitations. *See also supra,* Section III.B. Again, however, Micron asks this Court to wholly ignore the controlling case law.

Here, as in *Apex* and its progeny,[6] the claim pairs the term "circuit" with a description of its function and, thus, connotes sufficient structure to a POSITA. Przybylski Decl., ¶ 81. The '608 Patent claims recite a "command processing circuit," which is specifically configured to (1) receive and decode module control signals; (2) control the data path in accordance with module control signals and the module clock signal; (3) control at least one tristate buffer; and (4) determine an amount of delay for a data signal through the data path in response to a module control signal, the data path corresponding to each data/strobe signal line in the respective set of data/strobe signal lines. '608 Patent at claim 1; Przybylski Decl., ¶ 82. Here, structural

[6] *See, e.g.*, *Phenix Longhorn, LLC v. Wistron Corp.*, No. 2:17-cv-00711-RWS, 2019 WL 2568476, at *16 (E.D. Tex. Jun. 21, 2019) (finding that "circuit" or "circuitry" is neither a nonce term nor governed by §112, ¶ 6); *Intellicheck Mobilisa, Inc., v. Honeywell Int'l Inc.*, No. C16-0341JLR, 2017 WL 6550700, at *6 (W.D. Wash. Dec. 21, 2017) (same); *Realtime Data, LLC v. Rackspace US, Inc.*, No. 6:16-cv-00961 RWS-JDL, 2017 WL 2590195, at *15 (E.D. Tex. Jun. 14, 2017) (same); *Customedia Tech., LLC v. DISH Networks Corp.*, No. 2:16-cv-129-JRG, 2017 WL 568669, at *32 (E.D. Tex. Feb. 13, 2017) (same); *Cequent Performance Prod., Inc. v. Hopkins Mfg. Corp.*, No. 13-cv-15293, 2017 WL 371230, at *5 (E.D. Mich. Jan. 26, 2017) (same); *Technology Licensing Corp. v. Blackmagic Design Pty Ltd.*, No C 13-051854 SBA, 2016 WL 8902602, at *14 (N.D. Cal. Nov. 23, 2016) (same); *Intellicheck Mobilisa, Inc. v. Wizz Sys., LLC*, 173 F. Supp. 3d 1085, 1111 (W.D. Wash. 2016) (same); *Core Wireless Licensing S.A.R.L. v. LG Elec., Inc.*, No. 2:14-cv-0911-JRG-RSP, 2015 WL 6956722, *17 (E.D. Tex. Nov. 9, 2015) (same); *Acco Brands USA, LLC v. Comarco Wireless Tech., Inc.*, No. C 11-04378 RS, 2013 WL 843447, *15 (N.D. Cal. Mar. 6, 2013) (same); *Micro Motion, Inc. v. Krohne, Inc.*, No. 09CV10319-NG, 2011 WL 386837, at *12 (D. Mass. Feb. 3, 2011) (same); *P3 Intern. Corp. v. Unique Prods. Mfg. Ltd.*, No. 08 Civ. 5086 (DLC), 2009 WL 1424178, at *7 (S.D.N.Y May 21, 2009) (same); *RGB Sys., Inc. v. SP Controls, Inc.*, No. 04-6946 GPS (FMOx), 2005 WL 6225161, at *5 (C.D. Cal. Aug. 12, 2005) (same); *Inline Connection Corp. v. AOL Time Warner Inc.*, 302 F. Supp. 2d 307, 325-26 (D. Del. 2004) (same).

limitations are inherent to the claim language. A POSITA would understand the claims' requirement that the "command processing circuit" receive and decode module control signals conveys to a POSITA that the "command processing circuit" includes receiver circuits to perform the receiving. Przybylski Decl., ¶ 83. Similarly, the claims' requirement that the "command processing circuit" decodes the module control signals conveys to a POSITA that the "command processing circuit" include a decoder. *Id.* The claims' requirement that the command processing circuit controls a tristate buffer in the data path conveys to a POSITA that the "command processing circuit" includes a command signal driver to drive the signal controlling the tristate buffer in the data path. *Id.* These constraints ground the scope of the term.

The claims' description of how the "command processing circuit" interacts with other claimed components also imparts structure. For example, the express claim language makes clear that the "command processing circuit" must be capable of receiving module control signals from the module control device, as well as control the claimed tristate buffer. '608 Patent at claim 1. This conveys to a POSITA that the "command processing circuit" include a command signal driver to drive the signal controlling the tristate buffer into the data path. Przybylski Decl., ¶¶ 83-84.

The intrinsic written specification further teaches that the "ID control circuit 310 further includes a ***command processing circuit*** 640 that provides the received, decoded, and/or otherwise processed module control signals 330 to the DQ routing circuits 320 and the strobe routing circuit 620 either directly or after further processing, if needed." '608 Patent at 12:14-19 (emphasis added); *id*. at 12:19-26 (describing exemplary "received/decoded/processed module control signals" sent by the command processing circuit); Przybylski Decl., ¶ 86. Figure 6 confirms this structure as shown below.

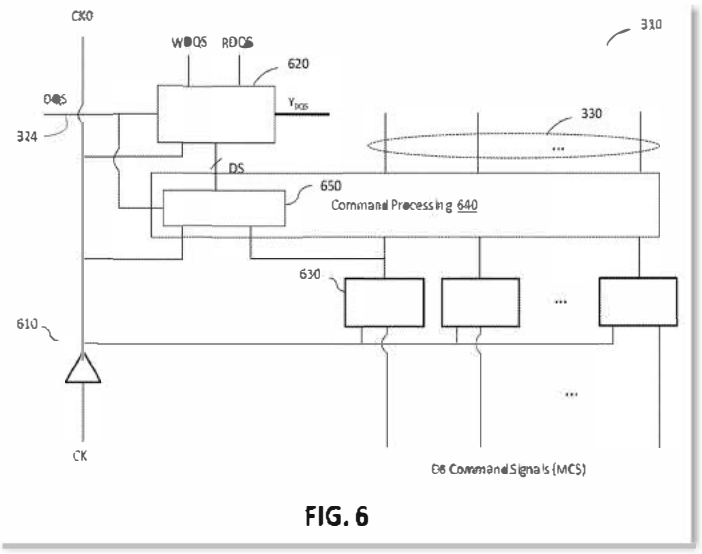


FIG. 6

'608 Patent at Fig. 6.

Figures 15 and 16 show tristate buffers 1520A/1630A and 1530B/1630B controlled by control signals ENA and ENB, respectively. These signals are generated and driven from within the command processing circuit. '608 Patent at Figures 6, 14-16, and 19, 10:50-11:7, 12:19-26; *see also* Przybylski Decl., ¶ 85. The details provided by the patent regarding how the "command processing circuit" interacts with other components—which Micron fails to address—conveys structure to a POSITA. *See Williamson*, 792 F.3d at 1351.

The two district court cases Micron cites are inapplicable here. Brief at 17 (citing *Limestone Memory Sys. LLC v. Micron Tech., Inc.*, No. 8:15-cv-00278-DOC, 2019 WL 6655273, at *18-19 (C.D. Cal. Sep. 11, 2019) and *Koninklijke Philips N.V. v. ZOLL Lifecore Corp.*, No. 2:12-cv-1369, 2015 WL 12781199, at *14 (W.D. Pa. Aug. 28, 2015)). First, those cases are not binding. Second, they each represent minority views. Finally, the cases are readily distinguishable—unlike the claims here, both cases rely on claimed circuitry that was completely unbound.

Because a POSITA would understand the claimed "command processing circuit" to

convey structure as described above, § 112, ¶ 6 does not apply. To the extent the Court finds the term subject to § 112 in contravention of case law and the intrinsic record, there is corresponding structure in the specification. *See* '608 Patent at Figures 3, 6, 11A, 11B, 12A, 12B, 14, 15, 16, 19; *see id.* at 10:50-11:2, 12:11-26, 14:57-17:54, 18:14-20, and 19:1-12 (reflecting embodiments for performing the claimed function); *see also* Przybylski Decl., ¶ 88.

IV. CLAIM CONSTRUCTION REGARDING THE '314 PATENT

The '314 Patent relates to devices and methods for improving the performance and/or memory capacity of memory modules in computer systems. '314 Patent at 1:46-49. At a high level, the claimed inventions permit increased memory density of memory devices to improve the performance and/or memory capacity of memory modules. *Id.* at 2:64-3:13.

A. "burst of data strobes" (Claims 1, 15, 25, and 28)

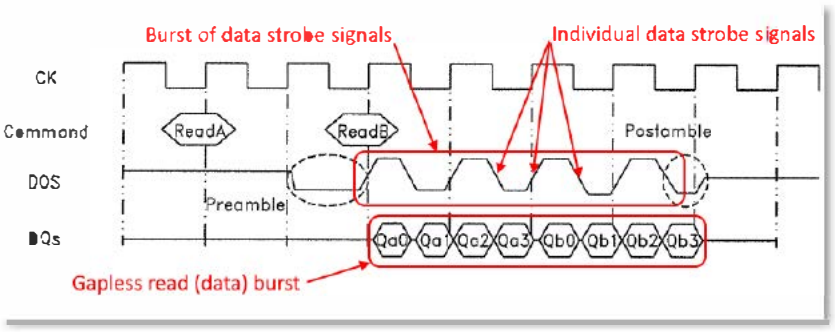
Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Not indefinite. In the alternative "strobe signals with successive rising and falling edges, each edge being associated with one or more data bits"[7]	Indefinite.

Micron challenges the validity of claims 1, 15, 25, and 28 by arguing the term "burst of data strobes" is indefinite. Micron's argument is meritless.

The '314 Patent specification teaches what is meant by "burst of data strobes." For example, the specification refers to data bursts, which are temporally consecutive values transmitted on a data bus. *See, e.g.*, '314 Patent at 3:17-4:30, 13:28-51; Fig. 7 (burst of four (data

[7] Netlist's alternative construction is amended from "a data bit" to "one or more data bits." *See* Przybylski Decl., ¶ 92. This change adds precision and does not impact the parties' positions. *Id.*

a) values (Qa0-Qa3) synchronized to four edges of a data strobe signal); Przybylski Decl., ¶¶ 96-98. Data strobe signal (DQS) lines carry data strobe signals. '314 Patent at 13:60-14:22, 14:41-56, 35:20-23; Przybylski Decl., ¶ 99. The specification also teaches that in DDR SDRAM, memory devices operate with data transfer protocol which surrounds each *burst of data strobes* with a pre-amble and a post-amble (as shown in Figures 6A and 6B). '314 Patent at 13:18-22. Turning to Figure 6A, a POSITA would understand a burst of data strobes as being strobe signals with successive rising and falling edges—that are used to capture the individual data values of the data bursts—between the pre-amble and post-amble, each edge being associated with one or more data bits. *See* Przybylski Decl., ¶ 100.



'314 Patent, Fig. 6A (annotated).

A POSITA's understanding would be further informed by the JEDEC standards for DDR2 memory systems, which are discussed in the '314 Patent's specification. Przybylski Decl., ¶¶ 39-41. The cited standards explain the (1) purpose and operation of strobe signals on DQS signal lines, (2) relationship between strobe signals and corresponding data values for both read and write memory operations, and (3) temporal relationship between data strobe signals on the DQS signal lines and the data values on the DQ lines. *Id.* at ¶¶ 101-103.

Instead of focusing on whether a POSITA would understand the meaning of the term "burst of data strobes," Micron argues that the term is allegedly indefinite because a strobe signal

line could *originate* from either two different memory devices, or a single memory device. According to Micron, the term "burst of data strobes" must take on two opposed meanings and, thus, the term is rendered completely unintelligible. Micron's argument is meritless.

First, the specific origin of a strobe signal line is irrelevant to a POSITA's ability to understand the term "burst of data strobes." For example, turning again to Figure 6A, regardless of where the data strobe signal (DQS) line originated from, a POSITA would readily be able to identify the burst of data strobes, which is circled above. *See* Przybylski Decl., ¶¶ 100, 106.

Second, though Micron argues that a strobe signal line can be formed in different ways, that does not mean that the term "burst of data strobes" must adopt two different meanings. For example, Figure 7 of the '314 Patent shows three different data strobe signal lines—one for strobe a, one for strobe b, and one for combined strobe. A POSITA would understand that the term "burst of data strobes" is correctly applied to each of those signal lines using the same meaning—expressly as shown in Figure 7. *See* Przybylski Decl., ¶¶ 106-107.

Finally, Micron's reliance on *Dow Chem. Co. v. Nova Chems. Corp*., 803 F.3d 620 (Fed. Cir. 2015) and *Teva Pharm. USA, Inc. v. Sandoz, Inc*., 789 F.3d 1335 (Fed. Cir. 2015) is misplaced. Those cases included claims requiring precise mathematical calculations to determine adherence to claim terminology, and thus infringement. Not so here. The identification of a burst of data strobes does not change depending on *how* a data strobe signal was formed, which distinguishes this case from *Dow* and *Teva*. At most, Micron's arguments suggest that "burst of data strobes" can be applied to different embodiments, but that does not render the term indefinite. *See Cywee Grp., Ltd. v. Huawei Device Co., Ltd*., No. 2:17-cv-00495 WCB-RSP, 2018 WL 6419484, at *15 (E.D. Tex. Dec. 6, 2018) ("Merely because a claim is drafted broadly and could cover a variety of methods does not automatically render a claim indefinite.").

B. The "Logic" Terms (Claims 1, 15, and 25)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Neither indefinite nor subject to § 112, ¶ 6.	This is a means-plus-function limitation. Function • For claim 1, "respond[ing] to the first/second memory command by providing first/second control signals to the circuitry" • For claims 15/25, "output[ting] first/second control signals to the circuitry . . . in response to the first/second read or write memory command" Corresponding Structure: Indefinite – no corresponding structure.

Claims 1, 15, and 25 recite "logic" terms without the word "means." Thus, § 112, ¶ 6 is presumed not to apply, and should not apply here for the following reasons.

First, the claims treat "logic" as a structural limitation. *See* Przybylski Decl., ¶ 112. Claim 1 recites that logic is "coupled to" circuitry and configured to provide control signals to the circuitry. "Logic" therefore denotes a physical structure in the '314 Patent claims. *Rodime PLC v. Seagate Tech., Inc.*, 174 F.3d 1294, 1303-04 (Fed. Cir. 1999) (finding that reciting location and interconnection of elements is a detailed recitation of structure).

Second, the specification confirms that "logic" denotes structure in the context of the asserted claims. *See* Przybylski Decl., ¶ 113. For example, the specification teaches that the claimed "logic" elements can be selected from a group of physical components consisting of "a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD)." '314 Patent at 7:5-10. Figure 9A also includes a diagram

of memory module 10 including electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 210, wherein the logic element is depicted as one of the physical components. *Id*. at Figure 9A, 16:36-39, 16:60-63; *see also Medtronic, Inc. v. Edwards Lifesciences Corp*., No. 11-1650 (JNE/JSM), 2013 WL 2147909, at *10 (D. Minn. May 16, 2013) ("[E]ach figure depicts the 'tensioning component' as a definite structure—as an identifiable part of the connector assembly. . . . It is not a generic term such as 'mechanism,' means,' 'element,' or device.'"). The specification also includes numerous other examples where logic is described as a physical, structural element. *See, e.g*., '314 Patent at 7:12-16, 9:25-51, 15:19-24, 17:50-55, 22:51-53, 34:42-67; Verilog examples 1-3 (describing physical hardware structures that perform logic functions); *see also* Przybylski Decl., ¶¶ 113-115.

Third, courts have consistently found that "logic" connotes sufficiently definite structure and is not a "nonce" or "functional" word that is subject to the limitations of § 112 ¶ 6. *See supra* Section III.B. This is consistent with extrinsic evidence, including dictionary definitions. *Id*.

Fourth, the asserted claims describe sufficient structure for logic for performing the claimed functions. *See* Przybylski Decl., ¶ 112. A POSITA would understand that the claimed logic is not an isolated and abstract device, but rather a concrete unit that fills multiple critical roles within the memory module. *Id*. at ¶ 115. In particular, the claims recite limitations wherein the logic must be a specific type of device capable of (1) receiving memory commands, (2) decoding and interpreting those commands, (3) generating the appropriate control signals at the appropriate time, and (4) communicating those control signals to the recited circuitry. *Id*. A POSITA would therefore understand that the claimed logic (1) includes physical structures such as receivers, decoders, registers, and drives to perform those claimed functions, and (2) exclude

other types of logic lacking those structures to perform the claimed functions. *Id*. Importantly, a term is not equivalent to "means" simply because such term may be broad and does not "call to mind a single well-defined structure." *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996). Thus, while not limited to a single embodiment, the claims recite sufficiently definite structure to avoid the ambit of § 112, ¶ 6.

Fifth, Micron's reliance on *Egenera,* 972 F.3d at 1375 and *MTD Products*, 933 F.3d at 1243 is inapposite for the same reasons as set forth above. *See supra* Section III.B.

Finally, even if the Court determines that "logic" is a means-plus-function term, the term should still be construed to encompass each of the structural embodiments disclosed in the '314 Patent for performing the claimed function. *See, e.g.*, '314 Patent at 7:5-10 (PLD, ASIC, FPGA, and CPLD devices), 7:12-16, 9:25-51, 15:19-24, 16:36-39, 16:60-63, 17:50-55, 22:51-53, 34:42-67, Figs. 5A-5D, 9A-9B, Verilog examples 1-3; Przybylski Decl., ¶ 117; *see also Creo*, 305 F.3d at 1346.

C. "overall CAS latency of the memory module" / "actual operational CAS latency of each of the memory devices[/of each of the plurality of memory integrated circuits]" (Claims 1, 15, 25, and 28)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. <u>In the alternative</u> "overall CAS latency of the memory module" means "the delay between: (1) the time when a command is sampled on the memory module, and (2) a time when the first piece of data is available at the data pins of the memory module" "actual operational CAS latency of each of the memory devices[/of each of the plurality of memory integrated circuits]" means "the delay between: (1) the time when a command	"overall CAS latency of the memory module" means "the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module" "actual operational CAS latency of each of the memory devices[/of each of the plurality of memory integrated circuits]" means "the delay between: (1) the time when a read command is executed by each of the memory devices[/each of the plurality of memory integrated circuits], and (2) the time when the first piece of data is made available at an output of each of the memory devices[/of

is executed by each of the memory devices[/each of the plurality of memory integrated circuits], and (2) a time when the first piece of data is available at the data pins of each of the memory devices[/of each of the plurality of memory integrated circuits]"	each of the plurality of memory integrated circuits]"

The dispute here is whether the disputed CAS latency terms only apply to read commands, or whether they apply to both read and write commands. Netlist's proposals are consistent with the plain and ordinary meaning of the CAS latency terms that applies to both read and write commands. Micron, on the other hand, attempts to improperly narrow the disputed terms to encompass read commands only. Micron's unjustified narrowing should be rejected.[8]

First, the language of the claims themselves support constructions that include both read and write commands. *See Biagro W. Sales, Inc. v. Grow More, Inc.*, 423 F.3d 1296, 1302 (Fed. Cir. 2005) ("[C]laim construction begins with, and remains focused on, the language of the claims."). For example, independent claim 15 applies the concept of an overall CAS latency to both read ***or write*** commands. *See, e.g.*, '314 Patent at 45:19-29; Przybylski Decl., ¶ 124.

Second, the '314 Patent specification supports Netlist's constructions including both read and write commands. For example, the specification teaches that "[t]he one-cycle time delay of certain such embodiments provides sufficient time for read ***and write data transfers*** to provide the functions of the data path multiplexer/***demultiplexer***." '314 Patent at 22:53-58 (emphasis added). Here, the time delays apply to both read data which are multiplexed onto the common DQ/DQS signal lines to the memory controller, and to ***write*** data which are ***demultiplexed*** onto the DQ/DQS signal lines to the memory devices. Przybylski Decl., ¶ 125. The specification also

[8] Contrary to what Micron argues, a POSITA would have been readily familiar with the concept of CAS latencies at the time of the Solomon invention. *See, e.g.*, Przybylski Decl., ¶ 121. As such, plain and ordinary meanings of the disputed CAS latency terms can be applied.

describes transfers ***between*** the memory controller and the memory module, and not just transfers ***from*** the memory module to the memory controller. '314 Patent at 22:43-45. A POSITA would understand the "between" language, which is inherently bidirectional, as referring to both read and write commands. Przybylski Decl., ¶ 126.

The specification also discloses Verilog code for certain embodiments of the invention. *See, e.g.*, '314 Patent, at col. 10-13, 25-29, 30-32. The Verilog code enables devices to allow read and write data to flow between the memory device and the memory controller. Przybylski Decl., ¶¶ 11-13. The detailed code uses the CAS latency ("cl") variables in both the case of a read command (*i.e.*, a signal of the form rd_cmd_cycx is active) and write command (*i.e.*, a signal of the form wr_cmd_cycx is active). '314 Patent at col. 27; Przybylski Decl., ¶¶ 129-131. The Verilog code described in the specification therefore teaches a POSITA that CAS latency in the context of the '314 Patent applies to both read and write commands. *Id*. Micron's proposals exclude these disclosed embodiments and should therefore be rejected. *SynQor, Inc. v. Artesyn Techs. Inc*., 709 F.3d 1365, 1378-79 (Fed. Cir. 2013) ("A claim construction that 'excludes the preferred embodiment is rarely, if ever, correct and would require highly persuasive evidentiary support.'").

Finally, Micron again attempts to impermissibly narrow terms without demonstrating a clear disavowal of claim scope in the intrinsic record. Instead, Micron relies exclusively on the DDR standards to argue that the disputed CAS latency terms must exclude write operations.[9] Brief at 26. But, as an initial matter, the claims recite distinct "*overall* CAS latency" and "*actual*

[9] Other extrinsic evidence also supports Netlist's construction. *See, e.g*., Przybylski Decl., ¶¶ 132-133 (citing Ex. D (Jacobs Article) at 16, which confirms that ***technically sound*** alternatives available to the JEDEC community in the early to mid-1990's included devices that "[e]xplicitly identify the CAS latency in the read ***or write*** command").

operational CAS latency" terms. Those terms are used by the '314 Patent, but not used by the JEDEC standards. *See, e.g.*, '314 Patent at 22:47-48, 22:60-61 (using "overall CAS latency" to refer to the latency of the memory module/system); *id.* at 25:25, 25:44-27:8 (implementing "actual operational CAS latency"); Przybylski Decl., ¶¶ 127-128, 134. Thus, Micron's complete reliance on the DDR standards in this context is inappropriate, and a POSITA would have interpreted the specific CAS latency terms in the '314 Patent claims as including write operations based on at least on the patent's teachings. *See, e.g.*, '314 Patent at 22:47-61; Przybylski Decl., ¶¶ 124-131.

Further, the DDR2 standard—which was repeatedly referenced in the '314 Patent specification's examples—support Netlist's interpretation of the disputed CAS latency terms. *See, e.g.*, '314 Patent at 22:58-62, 26:7-11, 29:16-20, 31:34-40, 36:36-38; Przybylski Decl., ¶¶ 134-141. For example, in the DDR2 standard, both the read latency (RL) and the write latency (WL) depend equivalently on the CAS latency (CL). Przybylski Decl., ¶¶ 134-141 (including further technical explanations); Ex. B (JESD79-2A) at 24. Thus, even the standards do not support Micron's narrow construction.

In short, Micron's proposed constructions contravene the intrinsic record, are too limiting, and should thus be rejected. The Court can adopt plain and ordinary meanings here. But if the Court determines that express constructions would be helpful, the terms should be construed as proposed by Netlist. Przybylski Decl., ¶¶ 123-128.

D. The "Circuitry" Terms (Claims 1, 15, 25, 28)

Plaintiff's Proposed Construction	Defendants' Proposed Construction
Plain and ordinary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. Neither indefinite nor subject to § 112, ¶ 6.	This is a means-plus-function limitation. Function: The claimed functions of the "circuitry" limitations are identified at Defendants' Exhibit 13. Corresponding Structure: Indefinite – no

	corresponding structure.

Again, Micron attempts to shoehorn a structural claim term into the confines of § 112, ¶ 6. But Micron's proposals should be rejected for the following reasons.

First, the claims treat "circuitry" as a structural limitation. *See* Przybylski Decl., ¶¶ 144-145. For example, claim 1 recites that the "circuitry" is coupled (1) between the plurality of N-bit wide ranks and the N-bit wide data bus; and (2) to the logic. The "circuitry" is further configured to (1) enable data transfers ***through*** the circuitry; and (2) add a predetermined amount of time delay for each data transfer. Thus, the claim language indicates that the term "circuitry" denotes a physical structure. *Inventio AG v. ThyssenKrupp Elevator Am. Corp.,* 649 F.3d 1350, 1358 (Fed. Cir. 2011) ("In past cases, we have concluded that a claimed 'circuit,' coupled with a description of the circuit's operation in the claims, connoted sufficiently definite structure to skilled artisans to avoid the application of § 112, ¶ 6.") (citing *Abacus*, 462 F.3d at 1355-56; *Linear Tech. Corp.*, 379 F.3d at 1320-21; *Apex Inc. v. Raritan Comp., Inc.*, 325 F.3d 1364, 1374 (Fed. Cir. 2003)); *see also Rodime*, 174 F.3d at 1303-04 (finding reciting location and interconnection of elements is a detailed recitation of structure).

Second, as set forth above, the Federal Circuit has repeatedly found that "circuit" and "circuitry" are not nonce terms invoking § 112, ¶ 6, and district courts have consistently followed suit. *See supra* at III.3 (citing cases).

Third, the '314 Patent provides sufficient structure for "circuitry" for performing the claimed functions. *See* Przybylski Decl., ¶¶ 146-150. A POSITA would understand that the claimed circuitry is not an isolated and generic circuit, but rather a concrete circuit unit that fills multiple critical roles within the memory module. *Id*. at ¶ 149. In particular, the claimed "circuitry" must be a specific type of circuitry that is capable of (1) receiving control signals; (2)

enabling transfers of bursts of data and strobe transfers between either of a plurality of ranks of memory devices and a memory controller at the full specified data rate in response to the control signals; (3) registering the data transfers, and (4) adding a predetermined time delay to each registered data transfer through the circuitry. *Id*. As would be understood by a POSITA, many different types of circuitry would not be capable of carrying out these functions, and the claimed circuitry would include structures such as registers, tri-state buffers, and wide data paths. *Id*.; *see also* '314 Patent at 22:38-53 (disclosing circuitry comprising combinatorial logic, registers, and logic pipelines). Importantly, a term is not equivalent to "means" simply because such term may be broad and does not "call to mind a single well-defined structure." *Greenberg,* 91 F.3d at 1583. Thus, while not limited to a single embodiment, the claims recite sufficiently definite structure to avoid the ambit of § 112, ¶ 6.

Fourth, Micron's reliance on *Limestone,* 2019 WL 6655273, at *18-19 and *Koninklijke,* 2015 WL 12781199, at *14 is inapposite for the reasons set forth above. *See supra* Section III.C.

Finally, even if the Court determines that "circuitry" is a means-plus-function term, in contravention of established caselaw and the intrinsic evidence here, the term should still be construed to encompass each of the embodiments disclosed in the '314 Patent for performing the claimed function. *See, e.g*., '314 Patent at 22:38-63 (circuitry including buffers comprising combinatorial logic, registers, and logic pipelines); Figures 9A-B, 10A-10B, 11A-11B, Verilog examples 1-3; *see also Creo*, 305 F.3d at 1346.

V. CONCLUSION

For the reasons set forth above, Netlist respectfully requests that the Court reject Micron's constructions and adopt Netlist's constructions for the disputed claim terms.

Dated: March 10, 2022

/s/ *Rex Hwang*

Paul J. Skiermont (TX Bar No. 24033073)
Steven Hartsell (TX Bar No. 24040199)
Jaime Olin (TX Bar No. 24070363)
Ryan A. Hargrave (TX Bar No. 24071516)
Michael D. Ricketts (TX Bar No. 24079208)
SKIERMONT DERBY LLP
1601 Elm St., Ste. 4400
Dallas, TX 75201
Phone: (214) 978-6600
Fax: (214) 978-6601
pskiermont@skiermontderby.com
shartsell@skiermontderby.com
jolin@skiermontderby.com
rhargrave@skiermontderby.com
mricketts@skiermontderby.com

Rex Hwang (CA Bar No. 221079)
SKIERMONT DERBY LLP
800 Wilshire Blvd., Ste. 1450
Los Angeles, CA 90017
Phone: (213) 788-4500
Fax: (213) 788-4545
rhwang@skiermontderby.com

J. Stephen Ravel (TX Bar No. 16584975)
Kelly Ransom (TX Bar No. 24109427)
KELLY HART & HALLMAN LLP
303 Colorado, Suite 2000
Austin, Texas 78701
Tel: (512) 495-6429
steve.ravel@kellyhart.com
kelly.ransom@kellyhart.com

Attorneys for Plaintiff
Netlist, Inc.

CERTIFICATE OF SERVICE

I hereby certify that on March 10, 2022, counsel of record who are deemed to have consented to electronic services are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(b)(1).

/s/ *Rex Hwang*